IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

1. (cancelled)

2. (cancelled)

3. (currently amended) A multi-cycle path analyzing method making an analysis of a multi-cycle path which can take two cycles or more for a signal to propagate from a starting point of the path to its end point among paths within a circuit to be analyzed, comprising:~~The multi-cycle path analyzing method according to claim 2,~~

making an analysis of a circuit to be analyzed in correspondence with a name of each element which includes a cell configuring the circuit to be analyzed, and/or a meaning and/or a relationship of a signal to a terminal of each element; and

making a multi-cycle path determination of whether or not a path from a starting point to an end point is a multi-cycle path by using a result of the analysis, and

wherein in the analysis of the circuit to be analyzed, circuit conversion for a multi-cycle path analysis in correspondence with the meaning of the signal to the terminal of each element is performed; and the multi-cycle path determination is made by using a result of the circuit conversion, and

wherein in the circuit conversion, circuit conversion such that a signal which can be converted into an enable signal to memory elements at the starting point and the end point of the path among signals to the terminal of the element is performed.

4. (currently amended) The multi-cycle path analyzing method according to claim 3, wherein

in the multi-cycle path determination, multi-cycle path determination is made depending on whether or not a value of ~~a~~ the memory element ~~can~~ possibly change based on a value of the enable signal to the memory elements at the starting point and the end point of the path.

5. (currently amended) The multi-cycle path analyzing method according to claim 4, wherein

~~in the multi-cycle~~the path ~~determination made based on the value of the enable signal, if all of paths between the starting point and~~ is determined to be a multi-cycle path if the end point of the path ~~are inactive for a path which is determined not to be a~~ is disabled at a time next to the time when the starting point of the ~~multi-cycle~~ path is enabled, or if all of the paths between the starting point and the end point of the path ~~is determined to be a~~ are inactive, in the multi-cycle path determination made based on the value of the enable signal.

6. (previously presented) The multi-cycle path analyzing method according to claim 3, wherein in the circuit conversion, circuit conversion such that a selection control signal to a selector which controls a setting of a value in the memory element at the starting point and/or the end point is converted into the enable signal is performed.

7. (currently amended) The multi-cycle path analyzing method according to claim 3, wherein in the circuit conversion, if a source of a clock which drives the memory element at the starting point and/or the end point is also ~~a~~ the memory element, circuit conversion such that ~~an~~ the enable signal for the memory element of the clock source is converted into the enable signal for the memory element at the starting point and/or the end point is performed.

8. (previously presented) The multi-cycle path analyzing method according to claim 3, wherein in the circuit conversion, circuit conversion such that a clock which drives the memory elements is converted into the enable signal by using clock gating information of a clock which drives the memory elements at the starting point and the end point of the path is performed.

9. (currently amended) The multi-cycle path analyzing method according to claim 3, wherein:

in the analysis of the circuit to be analyzed, memory elements within the circuit are classified into groups by the name of each element;

a reachable state of a finite state machine represented by each of the groups is calculated; and

the multi-cycle path determination is made by using a result of the calculation.

10. (currently amended) The multi-cycle path analyzing method according to claim ~~1~~3, wherein

in the analysis of the circuit to be analyzed, a restriction circuit corresponding to a condition is added to the circuit to be analyzed based on the condition for a relationship between a value setting signal for an external input terminal of the circuit and a value read signal from an external output terminal; and

the multi-cycle path determination is made for the circuit to be analyzed after the addition.

11. (currently amended) The multi-cycle path analyzing method according to claim ~~1~~3, wherein ~~a multi-cycle path restriction which straddles a memory element and can move is detected by making the multi-cycle path analysis for a path which straddles the memory element~~the path between which memory elements the multi-cycle path restriction can move to is detected between the starting point and the end point of the path based on the result of the multi-cycle path analysis.

12. (currently amended) The multi-cycle path analyzing method according to claim ~~1~~3, wherein:

in the analysis of the circuit to be analyzed, information required for circuit conversion for the multi-cycle path analysis is stored in correspondence with the meaning of the signal to the terminal of each element which includes a cell configuring the circuit; and

the multi-cycle path determination is made by using stored contents.

13. (cancelled)

14. (currently amended) A multi-cycle path analyzing apparatus making an analysis of a multi-cycle path which can take two cycles or more for a signal to propagate from a starting point of the path to its end point among paths within a circuit to be analyzed, comprising:~~The multi-cycle path analyzing apparatus according to claim 13,~~

a circuit converting unit performing circuit conversion for making a multi-cycle path analysis in correspondence with a meaning of a signal to a terminal of each element which includes a cell configuring the circuit; and

a multi-cycle path determining unit making a determination of a path from a starting point

to an end point is a multi-cycle path by using a result of the circuit conversion, and

wherein said circuit converting unit performs circuit conversion such that a signal which can be converted into an enable signal for memory elements at the starting point and the end point of the path among signals for the terminal of the element into the enable signal.

15. (currently amended) A program, which is used by a computer making an analysis of a multi-cycle path which can take two cycles or more for a signal to propagate from a starting of the path to its end point among paths within a circuit to be analyzed, for causing the computer to execute a process, the process comprising:

performing circuit conversion for making an analysis of a multi-cycle path in correspondence with a meaning of a signal to a terminal of each element which includes a cell configuring the circuit; ~~and~~

making a determination of whether or not a path from a starting point to an end point is a multi-cycle path by using a result of the circuit conversion; and

said circuit converting unit performs circuit conversion such that the signal which is converted into an enable signal for memory elements at the starting point and the end point of the path among signals for the terminal of the element into the enable signal.

16. (canceled)